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EXAMINER

PETRANEK, JACOB ANDREW

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/749,271	Applicant(s) HAMMARLUND ET AL.	
	Examiner Jacob Petranek	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 July 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-30 are pending.
2. The office acknowledges the following papers:
Specification, petitions, oath, drawings, abstract, and claims filed on 7/6/2004,
Oath filed on 10/26/2004.

Priority

3. No claim for priority has been made in this application.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Therefore, the limitation from claim 3 “wherein status information is latency, dependency, and resource conflict information” must be shown or the feature(s) canceled from the claim(s). None of the figures shows a scoreboard containing all this information. Claims 11-12, 15, 21-22, 25, and 29 also relate to the scoreboard storing latency, dependency, and resource conflict information.

Also, the limitation from claim 5 “wherein the replay system is implemented within a multiple channel processor” must be shown or the feature(s) canceled from the claim(s). None of the figures show a multi channel processor.

No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Specification

5. The disclosure is objected to because of the following informalities:
6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.
7. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-2, 4, and 7 are rejected under 35 U.S.C. §102(b) as being anticipated by Merchant et al. (U.S. 6,385,715).
10. As per claim 1:

Merchant disclosed an adaptive replay system comprising:

A staging unit to forward an instruction in a replay loop parallel to an execution unit (Merchant: Figure 1 element 139, column 5 lines 16-30)(The staging queues A-D.);

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A selector device coupled to said staging area to place said instruction in an optimal position within said replay loop (Merchant: Figure 1 elements 150 and 154, column 6 lines 7-25)(Elements 150 and 154 are combined to read upon a selector device. The replay queue loading controller determines if the instruction is to be placed in the staging queues E and F or in the replay queue. The optimal position for the instruction is based on its placement within either the staging queues or the replay queue.); and

A scoreboard coupled to said selector device to store status information for said instruction (Merchant: Figure 1 element 140, column 5 lines 50-59)(The scoreboard is coupled to the selector device, which is the checker and replay queue loading controller.).

11. As per claim 2:

Merchant disclosed the system of claim 1 wherein said staging unit is comprised of multiple stages (Merchant: Figure 1 element 139, column 5 lines 16-30)(The staging queues A-D.).

12. As per claim 4:

Merchant disclosed the system of claim 2 wherein said multiple stages are equivalent in number to a number of stages in said execution unit (Merchant: Figure 1 element 139, column 5 lines 16-30)(It's inherent that the stages are equal so that scheduled instructions can be matched with the checker for possible retirement.).

13. As per claim 7:

Merchant disclosed the system of claim 1 wherein said selector device is to

analyze at least one instruction per clock cycle to determine whether said at least one instruction has executed correctly (Merchant: Figure 1 element 150, column 6 lines 7-25)(The checker determines if the instruction has executed correctly.).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 3, 9-15, 18-23, 25-27, and 29-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant et al. (U.S. 6,385,715).

16. As per claim 3:

Merchant disclosed the system of claim 1 wherein said status information is latency (Merchant: Figure 1 element 154, and column 9 lines 1-24)(The replay queue loading controller checks to see if an instruction is going to be a short or long latency instruction. It would have been obvious to one of ordinary skill in the art at the time of the invention that this information could also be stored within the scoreboard. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.), dependency, and resource conflict information (Merchant: Figure 1 element 140, column 5 lines 50-59)(A resource conflict can be a register dependency because a resource the instruction needs is not available. This can be checked for within the scoreboard.).

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17. As per claim 9:

Merchant disclosed the system of claim 1 wherein said selector device places said instruction in said optimal position within said replay loop based on status information for said instruction stored in said scoreboard (Merchant: Figure 1 element 154, column 9 lines 1-24)(The optimal position is selected based on latency information from element 154. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that the latency information could have instead been stored within the scoreboard. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

18. As per claim 10:

Merchant disclosed the system of claim 9 wherein said selector device can move instructions at least one position relative to a current position to said optimal position in said replay loop (Merchant: Figure 1 element 154, column 9 lines 1-24)(The replay queue loading controller has the effect of moving instructions up in their current position by putting them into the staging queues. When put in the staging queues, they can bypass those instructions that have longer latencies.).

19. As per claim 11:

Merchant disclosed the system of claim 3 wherein said scoreboard stores latency and dependency information for said instruction when said instruction is first scheduled, and updates latency and dependency information for said instruction when said instruction is executed (Merchant: Figure 1 element 140, column 5 lines 50-59)(The

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dependency information is updated to show if data sources were correct or not.)

(Merchant: Figure 1 element 154, and column 9 lines 1-24)(The replay queue loading controller checks to see if an instruction is going to be a short or long latency instruction. It would have been obvious to one of ordinary skill in the art at the time of the invention that this information could also be stored within the scoreboard. It would have been obvious to one of ordinary skill in the art that the latency information of load instructions would be updated upon cache misses. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

20. As per claim 12:

Merchant disclosed the system of claim 3 wherein said scoreboard stores resource conflicts for said instruction when said instruction encounters a resource conflict during execution (Merchant: Figure 1 element 140, column 5 lines 50-59)(A resource conflict can be a register dependency because a resource the instruction needs is not available. This can be checked for within the scoreboard. A resource conflict inherently occurs during execution with the checker determining if the correct data sources were used.)

21. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Claim 13 additionally recites the following limitations:

A multiplexer having a first input, a second input, and an output (Merchant: Figure 1 element 116)(The MUX contains 3 inputs and one output. However, it would

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have been obvious to one of ordinary skill in the art that another MUX could be placed within the replay system to select between an instruction from the staging queues and from the replay queue. It would have been obvious to one of ordinary skill in the art that the replay MUX output would feed a 2-input, 1-output MUX that selects between the scheduler and the replay system. One of ordinary skill in the art would look to figure 6 and see that this is the implementation for multiple threads and could also be transferred to a system without multithreading capability. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the MUX could be modified to select between the scheduler and the replay system);

A scheduler coupled to said multiplexer first input (Merchant: Figure 1 element 114, column 3 lines 59-65);

An execution unit coupled to said multiplexer output (Merchant: Figure 1 element 118, column 4 lines 8-19);

A memory device coupled to said execution unit (Merchant: Figure 1 element 120, column 4 lines 8-19); and

A replay system having an output coupled to said second multiplexer input (Merchant: Figure 1 element 117, column 5 lines 16-30).

22. As per claim 14:

Claim 14 essentially recites the same limitations of claim 2. Therefore, claim 14 is rejected for the same reasons as claim 2.

23. As per claim 15:

Claim 15 essentially recites the same limitations of claim 3. Therefore, claim 15 is rejected for the same reasons as claim 3.

24. As per claim 18:

Claim 18 essentially recites the same limitations of claim 7. Therefore, claim 18 is rejected for the same reasons as claim 7.

25. As per claim 19:

Claim 19 essentially recites the same limitations of claim 9. Therefore, claim 19 is rejected for the same reasons as claim 9.

26. As per claim 20:

Claim 20 essentially recites the same limitations of claim 10. Therefore, claim 20 is rejected for the same reasons as claim 10.

27. As per claim 21:

Claim 21 essentially recites the same limitations of claim 11. Therefore, claim 21 is rejected for the same reasons as claim 11.

28. As per claim 22:

Claim 22 essentially recites the same limitations of claim 12. Therefore, claim 22 is rejected for the same reasons as claim 12.

29. As per claim 23:

Merchant disclosed a method of processing a computer instruction in a replay loop comprising:

Analyzing multiple instructions from a staging unit (Merchant: Figure 1 element 139, column 5 lines 16-30)(There are multiple instructions within the staging unit that

will be analyzed to see if they correctly executed or not.);

Checking a scoreboard for latency information for each of said multiple instructions (Merchant: Figure 1 element 154, column 9 lines 1-24)(The replay queue loading controller checks to see if an instruction is going to be a short or long latency instruction. It would have been obvious to one of ordinary skill in the art at the time of the invention that this information could also be stored within the scoreboard. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.);

Checking for dependency information for each of said multiple instructions (Merchant: Figure 1 element 140, column 5 lines 50-59);

Checking said scoreboard for resource conflicts for each of said multiple instructions (Merchant: Figure 1 element 140, column 5 lines 50-59)(A resource conflict can be a register dependency because a resource the instruction needs is not available. This can be checked for within the scoreboard.);

Determining an optimal position for each of said multiple instructions in said replay loop (Merchant: Figure 1 element 154, column 6 lines 7-25)(The replay queue loading controller determines if the instruction is to be placed in the staging queues or in the replay queue. The optimal position for the instruction is based on its placement within either the staging queues or the replay queue.); and

Moving each of said instructions to said optimal position in said replay loop (Merchant: Figure 1 element 154, column 6 lines 7-25)(The replay queue loading controller determines if the instruction is to be placed in the staging queues or in the

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replay queue. The optimal position for the instruction is based on its placement within either the staging queues or the replay queue.).

30. As per claim 25:

Claim 25 essentially recites the same limitations of claims 3 and 9. Therefore, claim 25 is rejected for the same reasons as claims 3 and 9.

31. As per claim 26:

Claim 26 essentially recites the same limitations of claim 10. Therefore, claim 26 is rejected for the same reasons as claim 10.

32. As per claim 27:

Claim 27 essentially recites the same limitations of claim 23. Therefore, claim 27 is rejected for the same reasons as claim 23.

33. As per claim 29:

Claim 29 essentially recites the same limitations of claims 3 and 9. Therefore, claim 29 is rejected for the same reasons as claims 3 and 9.

34. As per claim 30:

Claim 30 essentially recites the same limitations of claim 10. Therefore, claim 30 is rejected for the same reasons as claim 10.

35. Claims 5-6 and 16-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant et al. (U.S. 6,385,715), in view of Merchant et al. (U.S. 6,163,838), herein referred to as 838.

36. As per claim 5:

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Merchant disclosed the system of claim 2.

Merchant failed to teach wherein said adaptive replay system is implemented within a multiple channel processor.

However, 838 disclosed wherein said adaptive replay system is implemented within a multiple channel processor (Merchant: Figure 3 element 50, column 5 lines 59-65).

Merchant is a continuation of 838. The advantage of using multiple channels is that performance will be increased by being able to execute additional instructions per cycle. Thus, it would have been obvious to one of ordinary skill in the art to look at 838 for additional details and find that the processor can include multiple channels.

37. As per claim 6:

Merchant disclosed the system of claim 5.

Merchant failed to teach wherein said selector device is to place said instruction in said optimal position within said replay loop, from a first channel to a second channel, based on status information for said instruction stored in said scoreboard.

However, it would have been obvious to one of ordinary skill in the art that multiple channels, or execution units could have the same functionality, such as an integer unit. It also would have been obvious to one of ordinary skill in the art that a replayed instruction could be scheduled to be executed on either integer unit. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the replayed instruction could change from a first channel to a second channel based on status information, which would tell that the instruction is to be replayed.

38. As per claim 16:

Claim 16 essentially recites the same limitations of claim 5. Therefore, claim 16 is rejected for the same reasons as claim 5.

39. As per claim 17:

Claim 17 essentially recites the same limitations of claim 6. Therefore, claim 17 is rejected for the same reasons as claim 6.

40. Claims 8, 24, and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant et al. (U.S. 6,385,715), in view of Topham et al. (U.S. 6,944,853).

41. As per claim 8:

Merchant disclosed the system of claim 7.

Merchant failed to teach wherein said selector device analyzes 3 instructions per clock cycle.

However, Topham disclosed wherein said selector device analyzes 3 instructions per clock cycle (Topham: Figure 1 elements 14-18, column 3 lines 25-42)(The combination of Topham and Merchant results in three execution units that are processing instructions per clock cycle. It would have been obvious to one of ordinary skill in the art at the time of the invention that the replay unit must add stages to keep track of the instructions from the new execution units and therefore analyzes 3 instructions per clock cycle to see if any of them can retire.).

The advantage of adding additional execution units is that it will increase the performance of the processor by executing additional instructions per cycle. The advantage of increased performance would have motivated one of ordinary skill in the art to implement additional execution units on the processor of Merchant. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add additional execution units for the advantage of increased performance.

42. As per claim 24:

Claim 24 essentially recites the same limitations of claim 8. Therefore, claim 24 is rejected for the same reasons as claim 8.

43. As per claim 28:

Claim 28 essentially recites the same limitations of claim 8. Therefore, claim 28 is rejected for the same reasons as claim 8.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Grochowski et al. (U.S. 6,035,389), taught scheduling instructions with different latencies.

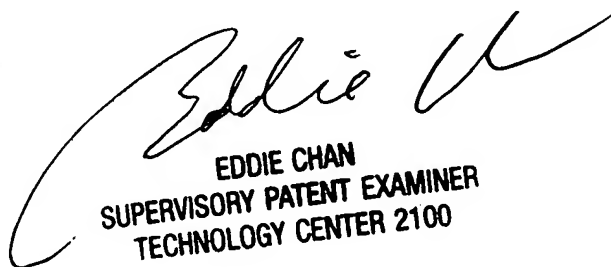
Merchant et al. (U.S. 6,094,717), taught a processor with a replay system that has two checkers to determine if instructions are to be replayed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
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